Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1-31. (Canceled)

32. (Currently Amended) A sequential read-out circuit comprising:

a first sample and hold circuit that includes a first sampling switch and a first sampling capacitor, the first sampling capacitor having a first and a second electrode;

a first photocell in an array of photocells, the first photocell comprising a first read switch and a first photodiode, the first read switch being operable to couple the first photodiode to the first electrode of the first sampling capacitor; and

an amplifier having a positive input terminal coupled to a reference voltage, the amplifier configured for operation in one of a unity gain mode and a charge transfer mode, wherein when operating in the unity gain mode, the first sampling switch is operable to couple the second electrode of the first sampling capacitor to a negative input terminal of the amplifier, thereby placing the second electrode of the first sampling capacitor at a voltage level equal to the reference voltage;

a second sample and hold circuit that includes a second sampling switch and a second sampling capacitor, the second sampling capacitor having a first and a second electrode;

a second photocell in an array of photocells, the second photocell comprising a second read switch and a second photodiode, the second read switch being operable to couple the second photodiode to the first electrode of the second sampling capacitor; and

wherein the first sampling switch is operable to uncouple the second electrode of the first sampling capacitor from the negative input terminal of the amplifier and the second sampling switch is operable to couple the second electrode of the second sampling capacitor to the negative input terminal of the amplifier, thereby placing the second electrode of the second sampling capacitor at the reference voltage.

33. (Canceled)

34. (Previously Presented) The sequential read-out circuit of claim 32, further comprising a first integration capacitor coupled between the negative input terminal of the amplifier and an output terminal of the amplifier whereby the amplifier is configured when placed in the charge transfer mode of operation, to provide a first voltage gain that is referenced to the voltage reference.

35. (Previously Presented) The sequential read-out circuit of claim 34, further comprising a first switching element having a first electrode coupled to the first integration capacitor and a second electrode coupled to the output terminal of the amplifier, the first switching element being operable to selectively couple the first integration capacitor to the output terminal of the amplifier.

36. (Previously Presented) The sequential read-out of claim 35, further comprising a second switching element having a first electrode coupled to a shift voltage and a second electrode coupled to the output terminal of the amplifier, the second switching element being operable to set the output terminal of the amplifier at the shift voltage.

37. (Previously Presented) The sequential read-out circuit of claim 34, further comprising a second integration capacitor selectively coupled between the negative input terminal of the amplifier and the output terminal of the amplifier whereby the amplifier is configured when placed in the charge transfer mode of operation, to provide a second voltage gain that is referenced to the reference voltage.

38. (Previously Presented) The sequential read-out circuit of claim 37, further comprising a third switching element having a first electrode coupled to the second integration capacitor and a second electrode coupled to the output terminal of the amplifier, the third switching element being operable to selectively couple the second integration capacitor to the output terminal of the amplifier.

39-45. (Canceled)

46. (Currently Amended) The sequential read-out circuit of claim 33 wherein the ~~same~~ amplifier is selectively coupled (a) between the negative input terminal of the amplifier and the second electrode of the first sampling capacitor, and (b) between the ~~same~~ negative input terminal of the amplifier and the second electrode of the second sampling capacitor.

47. (Currently Amended) The sequential read-out circuit of claim 32 wherein, when operated in the unity gain mode, the first electrode of the first sampling capacitor is coupled to a voltage V_{light} generated by the first photodiode and the second electrode of the first sampling capacitor is placed at the reference voltage; and when operated in the charge transfer mode, the amplifier provides a first output voltage ~~in response to a first input voltage ($V_{light} - V_{reset}$) stored in the first sampling capacitor, the first output voltage~~ constituting a read-out of the first photodiode.

48. (Currently Amended) The sequential read-out circuit of claim 47, further comprising:

a second sample and hold circuit comprising a second sampling capacitor; and wherein when operated in the charge transfer mode, the amplifier provides a second output voltage ~~in response to a second input voltage ($V_{light} - V_{reset}$) stored in the second sampling capacitor, the second output voltage~~ constituting a read-out of the second photodiode.